What is claimed is:

1. A semiconductor connection comprising:

at least two active areas;

an electrically conductive doped channel providing an electrical connection between said at least two active areas; and

a first conductive layer disposed over a first portion of said electrically conductive channel; and

a second conductive layer disposed over a second portion of said electrically conductive channel wherein said first and second conductive layers are spaced apart from one another.

2. The semiconductor connection of claim 1 wherein said first and second conductive layers are silicide layers.

3. The semiconductor connection of claim 1 wherein said electrically conductive doped channel comprises:

a first doped channel area adjacent to a first one of said at least two active areas;

a second doped channel area adjacent to a second one of said at least two active areas; and

a channel block structure disposed in between said first doped channel area and said second doped channel area.

4. The semiconductor connection of claim 3 wherein said first doped channel area, said second doped channel area, and said channel block structure have a same conductivity type.

5. The semiconductor connection of claim 3 wherein said at least two active areas have a first doping concentration and said channel block structure has a second doping concentration, said second doping concentration being less than said first doping concentration.

6. A method of making reverse engineering difficult comprising the steps of;

forming an electrically conductive doped channel between at least two active regions;

disposing a first conductive layer over a first portion of said electrically conductive doped channel; and

disposing a second conductive layer over a second portion of said electrically conductive doped channel wherein said first conductive layer and said second conductive layer are spaced apart from one another.

7. The method of claim 6 wherein said step of forming an electrically conductive doped channel further comprises the step of creating a channel block structure within said electrically doped conductive channel, wherein said channel block structure, said electrically conductive doped channel and said at least two active regions are of the same conductivity type.

8. The method of claim 7 wherein said channel block structure is created using a smaller dopant concentration than a dopant concentration used to create said at least two active regions.

9. The method of claim 6 wherein said first and second conductive layers are silicide layers.

10. A method of protecting an integrated circuit design comprising the steps of:

defining edges of a conductive layer for a non-conducting channel; and

placing edges of a conductive layer for a conducting channel in the same relative location as said edges of said conductive layer for said non-conducting channel.

11. The method of claim 10 wherein said conductive layer is silicide.